Analysis and Design of High gain Low Power Fully Differential Gain-Boosted Folded-Cascode Op-amp with Settling time optimization

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ABSTRACT

This paper presents the analysis and design of high speed, high gain fully differential operational amplifier (opamp). Both the main op-amp and the boosting op-amp are fully differential folded-cascode. The main op-amp has a switched capacitor common mode feedback circuit. Two fully differential folded-cascode op amps with continuous-time CMFBs are used as auxiliary op amps to increase the open-loop gain of the main op amp. Common mode feedback (CMFB) is used to stable the designed op-amp against temperature. This design has been implemented in 0.18µm UMC mixed signal CMOS Technology using Cadence. Spectre simulation shows that the op-amp has the DC gain of 112dB and the unity gain bandwidth of 1.15GHz.

Keywords **- Boosting amplifier, Cadence, CMFB, folded cascode, fully differential op-amp.**

I. INTRODUCTION

In high performance analog integrated circuits, such as switch-capacitor filters, delta-sigma modulators and pipeline A/D converters, op amps with very high dc gain and high unity-gain frequency are needed to meet both accuracy and fast settling requirements of the systems [1]. Analog and digital circuit integrates onto a single die to reduce system costs, but noisy digital circuit degrades analog performance due to noise injection through power distribution network or the substrate. Fully differential analog signal processing is one of the most important techniques that reduce the problems associated with noise coupling [2]. The fully differential technique doubles the maximum signal swing in the circuit effectively. The op-amp as the most important analog system building block has had to adopt the fully differential design technique. Active cascode gain-boosting technique can be used to increase the dc gain of an operational amplifier without degrading its high frequency performance. In 1997, D. Flandre proposed synthesis of cascode CMOS stages using g_m / I_d method, unfortunately, the existence of pole-zero doublet will unfavorably affect the settling performance of the gain-boosted op amp [3] and the effort of pushing up the doublet can raise stability problem [4]. For high gain, the architecture of a single stage amplifier with gain-boosted amplifier is a nice choice compare to telescopic topology. However, the folded-cascode topology requires more power, but it offers large output swing and has good performance on common mode input range [5]. Generally, speed and accuracy are two of the most important properties of operational amplifier & they are determined by the settling behavior of operational amplifiers. Fast settling requires a high unity-gain frequency and a single-pole settling behavior or the op amp, whereas accurate settling requires a high dc gain. Satisfying both speed and accurate is difficult with short-channel CMOS processes, since the output impedance of the device is limited [6]. So it is good to use a folded-cascode structure with gain-boosted amplifier in the sample and hold stage. This paper describes the analysis and the design of fully differential gain-boosted op-amp for 10 bit pipelined ADC. The organization of this paper is as follows: the design of the gain-boosted amplifier is explained in section II and the circuit implementation with 0.18µm CMOS process is presented in section III. In section IV, the simulation results are given and discussed .The conclusions are presented in section V.

II. THE DESIGN OF THE GAIN-BOOSTED AMPLIFIER

The design of the gain-boosted amplifier is illustrated in Fig.1. [7]. M0 and M1 form the main cascode amplifier. A is a gain-boosted amplifier. Gate of M1 is driven by A and forces the voltage at the drain of M0 and Vref to be equal. Because of the gain-boosted amplifier, voltage variations at the output will affect the voltage at the drain of M0 to a lesser extent variations. As a result, the output resistance is almost A times larger than that of a regular cascode. The output resistance Rout is given as:

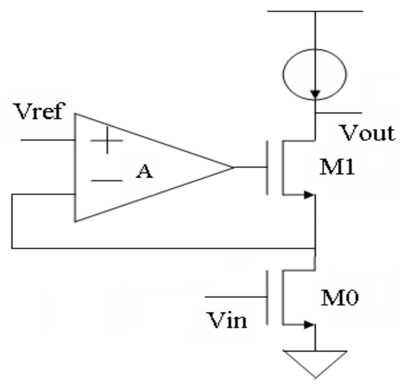

Fig.1. design of the gain-boosted amplifier

$$Rout = (g_{m2}r_{o1}(A+1)+1)r_{o1} + r_{o2} \quad (1)$$

According to R_{out}, the DC gain is:

$$A_{total} = g_{m0}r_{o0}(g_{m1}r_{o1}(A+1)+1) + g_{m0}r_{o1} \quad (2)$$

And the DC gain of the amplifier without gain boosting is:

$$A_{total} = g_{m0}r_{o0}(g_{m1}r_{o1}+1) \quad (3)$$

The gain boosting technology makes the DC gain of the circuit increasing several orders of magnitude.

III. CIRCUIT IMPLENTATION

1. DESIGN OF THE MAIN AMPLIFIER AND GAIN BOOSTING AMPLIFIER

For high gain designs, two-stage configuration might be the appropriate choice; however, the speed of this configuration is the bottleneck. In this design, a fully differential folded cascode that has two fully differential folded cascode boosting amplifiers has been implemented as shown in Fig.2. In order to achieve desired phase margin, two compensation capacitors C_c are connected as shown in Fig. 1.In the design process, NMOS transistors give about 4 times better transconductance compared to the same size PMOS transistors; this motivates us to reduce the number of PMOS transistors as much as possible. Since low common mode input is desired to avoid extra digital power consumption due to big PMOS switches, the input differential pair of the opamp was chosen to be PMOS transistors. It has a switched capacitor CMFB circuit that is active when the opamp is in the holding mode and a continuous time CMFB that is active when the opamp is in the sampling mode [8]. The boosting amplifiers have a continuous time CMFB circuits. The boosting amplifiers are of two types: the AN gain boosting amplifier has an NMOS differential input stage, while the AP has a PMOS differential input stage. The ideal effect of the auxiliary op amp is to increase the output impedance of the main op amp by auxiliary times so as to improve the dc gain of the main op amp [9]; at the same time, the dominant pole of the main opamp is pushed down by auxiliary opamp.

A well-known bandwidth constraint for the gain boosting amplifier is given in [10] as

$$\beta.\omega_u < \omega_{uGB} < \omega_{SP} \quad (4)$$

where β and ω_u are the feedback factor and the unity gain frequency of the main amplifier, respectively; ω_{uGB} and ω_{SP} are the unity gain frequency of the gain booster and the pole frequency at the source of the cascode transistor in the main amplifier, which is most probably the second pole, as well. In fact, the gain-boosting technique can potentially raise two significant problems for the time-domain performance of the gain-boosted op amp, i.e. doublet and instability. The PMOS type gain boosting amplifier, AP is shown in Fig.3. It is very similar to the main opamp with the exception that it does not have boosting amplifiers and the input differential stage is of NMOS transistors. The AN boosting amplifier is the same as the PMOS type with the exception that a PMOS differential input stage is used.

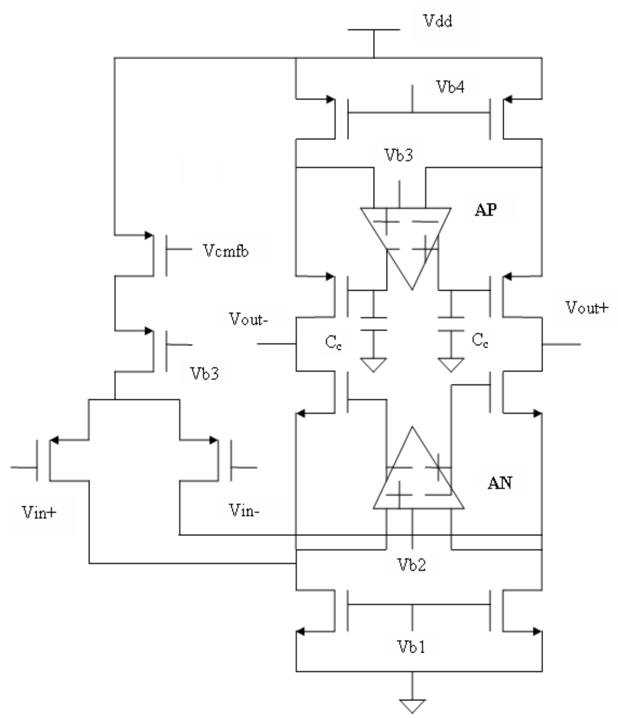

Fig.2. fully differential folded cascaded op-amp with fully differential gain-boosted amplifiers.

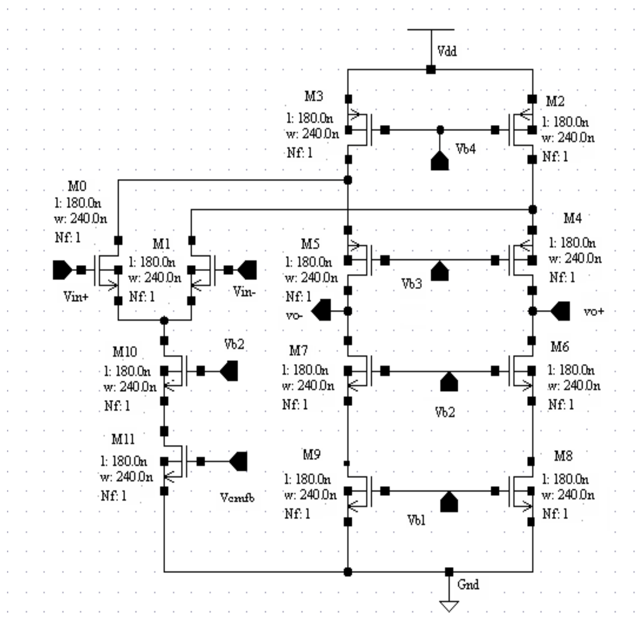

Fig.3. fully differential gain-boosted amplifier (AP).

2. DESIGN OF CMFB CIRCUIT

Fully differential opamp has much advantage, for example, greater output swing, avoid mirror poles eliminating even-order distortion and reject noise from the substrate, it has a drawback that it must have a common-mode feedback (CMFB) circuit. The CMFB circuit will enable the op amp to have a common mode output voltage that is immune to variations in the process as well as temperature. It is often the most difficult part of the op amp to design [11]. CMFB circuits can be divided into two general categories: switched-capacitor CMFB (SC-CMFB) circuits and continuous-time CMFB circuits. Compare to continuous time CMFB, SC-CMFB consumes less power. Because the opamp is used in sample and hold circuit, nonoverlapping phase clocks are available. The SC-CMFB is adopted which is shown in Fig.4.

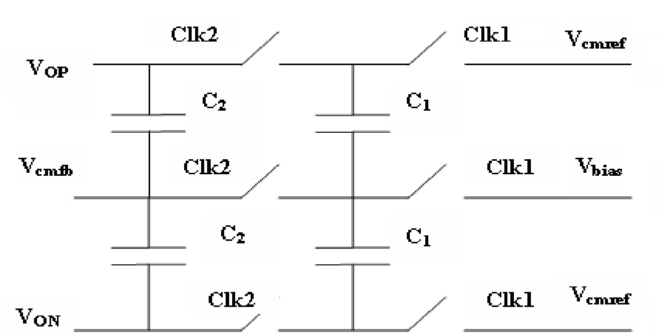

Fig.4.switched capacitance common mode feedback circuit

It consists of four capacitors and six switches. The size of the capacitors should be chosen carefully so that they will not over-load the main op-amp. During clock phase 1, c1 is charged to $V_{cmvref} - V_{bias}$ and capacitors C_2 and C_1 generate the control voltage V_{cmfb}, level shifting the average output voltage by $V_{cmvref} - V_{bias}$. During clock phase 2, C_1 and C_2 are connected in parallel. The DC voltage of C_2 is decided by C_1 and refreshed after every phase 2 period.

The output of each boosting amplifier does not need high swing, thus, a continuous time CMFB circuit is used [12]. The advantage of the continuous time CMFB is that its speed is fast. The first step is to design the boosting amplifier without the CMF'B circuit, but the common mode output should achieve an expectation voltage. Once this is finished, the CMFB circuit can be used. The CMFB circuit for gain boosting amplifier AP is shown in Fig.5. For gain boosting amplifier AN CMFB circuit is similar to the one of AP except that the input differentia pair is of NMOS transistors.

The main op amp and gain boosting amplifiers use the same bias circuit, as shown in Fig.6. Wide swing cascode current mirror is used to bias the circuit. These bias voltages will enable those transistors of main opamp and boosting amplifiers to work in saturation region.

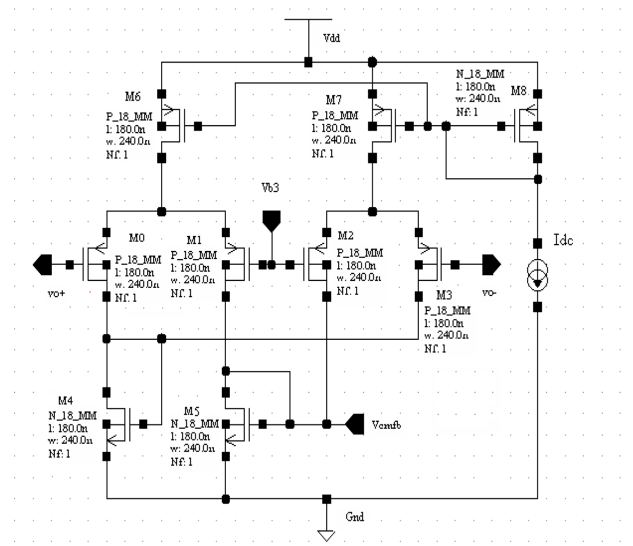

Fig.5. CMFB circuit for gain boosting amplifier AP.

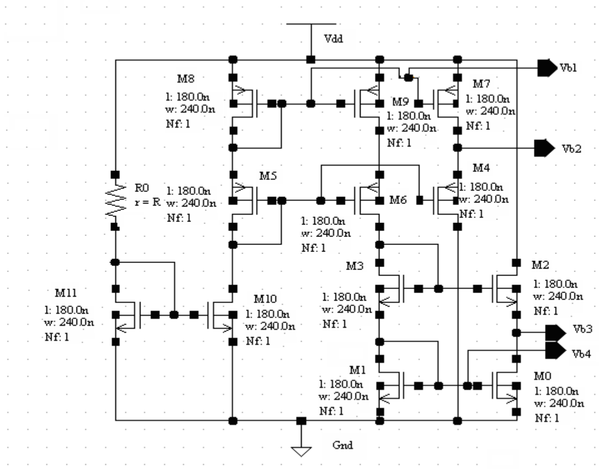

Fig.6. wide swing cascode current mirror circuit

IV. SIMULATION RESULTS

A single stage fully differential gain-boosted folded-cascode op amp is designed with the design process described above, and implemented in 0.18µm process with 1.8V power supply and simulated with Cadence Spectre. The load capacitance is 1pF. In Fig.7 AC simulation shows that the main amplifier has a dc gain of more than 138.9dB. The phase margin is 55^0. The unity GBW is 992.9MHz.

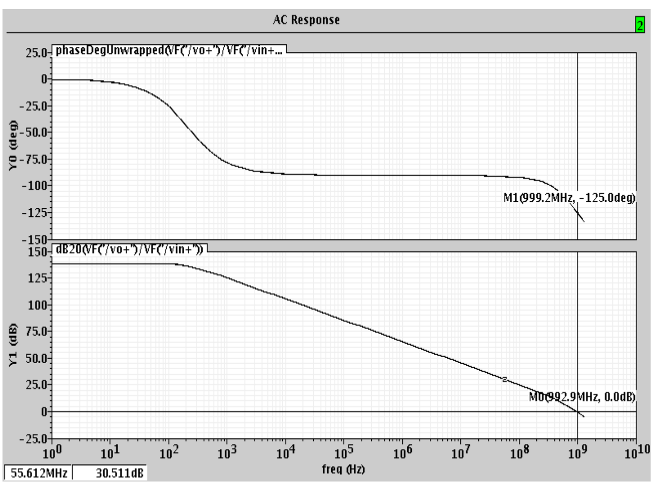

Fig.7. gain and phase response of folded cascode opamp.

1. SETTLING RESPONSE ANALYSIS

To understand the settling performance of the opamp, the step response is simulated by a closed-loop configuration shown in Fig. 8. Here, the load capacitor C_L is lpF. In order to achieve desired phase margin, two compensation capacitors C_c are connected as shown in Fig. 1. Sweeping the C_c, from 0.1pF to 1.2pF during transient simulation, the optimal C_c is found to be 0.4pF. When C_c is 0.4pF, the corresponding differential step response of the gain-boosted op amp is shown in Fig. 9.

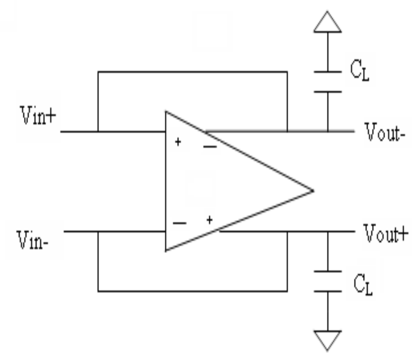

Fig.8. configuration for simulating the step response

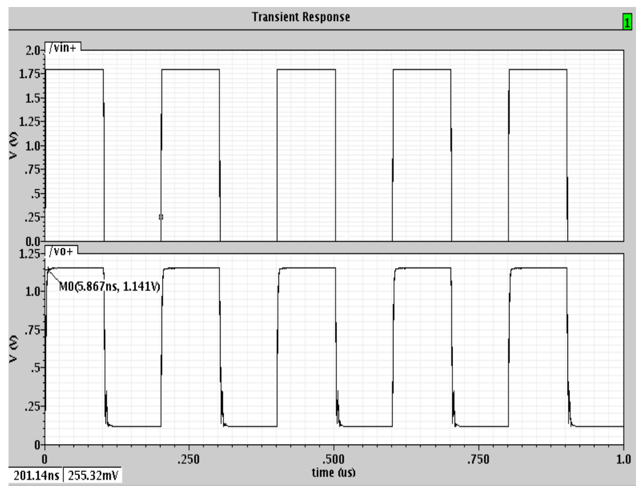

Fig.9. step response of proposed folded-cascode opamp.

V. CONCLUSION

Design and simulation of fully differential amplifier with gain boosting technology is presented in this paper. The gain-boosted amplifier is also implemented by folded cascode amplifier technique. Based on 0.18µm CMOS process, it has good performance, with a DC gain of 138.9dB and a unity gain bandwidth of 992.9MHz. Care has been taken in selection of the current values in both the cascode device and the gain boost device to ensure good settling time performance while maintaining the gain and bandwidth of the opamp. The simulation results show that the slow settling component arising from the pole-zero doublet due to gain-boosting technique is avoided and the method provides a simple and robust scheme of gain-boosted op amp optimization in terms of settling performance. The designed op-amp fulfills the stringent specifications of sample and hold stage of pipelined A/D converter with minimal additional power consumed. Present results are compared and improvement is observed as shown in Table 1.

Table 1: Comparison of present results with earlier reported work.

Ref.	Techno -logy (CMOS)	Gain (dB)	UGB (MHz)	Settl-ing time (ns)	Power Dissip ation (mW)
[6]	1.6µm	95 dB	116 MHz	61.5	52
[7]	0.35µm	129 dB	161 MHz	23.5	3.89
Present results	0.18µm	138.6 dB	999 MHz	5.86	3.13

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